Victor WOELFFEL

Final-year engineering student at Télécom Paris seeking a six-month internship from March 2027. Interested in processor architecture, embedded systems and artificial intelligence.

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Education

Télécom Paris – Institut Polytechnique de Paris *Sep. 2023 – Present*
Master of Science in Engineering, SE track *Expected Dec. 2027*
Exchange: Polytechnique Montréal, Canada (Aug. 2026 – Jan. 2027)

– *Embedded Systems:* processor design, assembly, memory organization, simulation and verification.

– *VLSI Integrated Circuits:* CMOS, RTL, VHDL, digital synthesis, placement and verification.

– *Reinforcement Learning:* MDPs, Q-learning, policy evaluation and learning-based agents.

Professional Experience

Emerton Data *Mar. 2026 – Aug. 2026*
Data Science Consultant Intern *Paris, France*
– Developed AI agents for structured technical protocols with Microsoft Copilot Studio, and worked on simulation optimization with Gurobi and Docker.

Capgemini Engineering – B-Reality *Sep. 2025 – Feb. 2026*
Research & Development Intern *Meudon, France*
– Developed and evaluated real-time EEG classification models for a VR rehabilitation system, reaching approximately 95% accuracy with inference below 10 ms per cycle.
– Co-first author of an IEEE conference paper (2026) comparing and optimizing c-VEP classification approaches.

Hands-on Projects

RISC-V Program Simulation and Custom Processor Design
– Decoded and simulated a RISC-V assembly program. Designed a custom 16-bit CPU and ISA with pipelining, hazard handling and forwarding; validated execution through architectural tests.

FPGA Memory Controller – Avalon Interface
– Designed an Avalon-compliant memory controller in SystemVerilog and verified it on an FPGA board, applying RTL interface design and hardware validation.

Reinforcement Learning Agent for a Strategy Game
– Implemented a Q-learning agent in Python with PyTorch and Gymnasium, working on state/action representations, exploration and policy evaluation.

Leadership Experience

Vice-President – Télécom Gaming Club *Jun. 2024 – Jun. 2025*
– Coordinated 20 members and organized a public tournament with over 100 participants.

Technical Skills and Languages

Hardware: SystemVerilog, VHDL, FPGA, RTL, RISC-V, processor simulation, Avalon
Programming and ML: Python, PyTorch, NumPy, Q-learning; C and Rust coursework
Tools: Linux, Git, Docker, Gurobi
Languages: French (native), English (B2.2)